The following listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) An input buffer circuit comprising [[;]]:

a first input buffer for receiving an external input signal applied from an external of a semiconductor device;

a second input buffer for receiving an external reference voltage and the external input signal; and

a control means for generating a control signal selecting the first input buffer or the second input buffer,

wherein the first input buffer operates when the control signal is a signal having a first level, and the second input buffer operates when the control signal is a signal having a second level,

wherein the control signal [[ENABLEs]] enables the first input buffer when a potential level of the external input signal is smaller than a first reference voltage or larger than a second reference voltage, and the control signal [[ENABLEs]] enables the second input buffer when the potential level of the external input signal is located between the first reference voltage and the second reference voltage.

2. (Original) The input buffer circuit according to claim 1, wherein the first input buffer is a CMOS buffer, and the second input buffer is a differential input buffer.

3. (Currently Amended) An input buffer circuit comprising:

a first input buffer for receiving an external input signal applied from an external of a semiconductor device;

a second input buffer for receiving an external reference voltage and the external input signal; and

a control means for selecting the first input buffer when a mode of the semiconductor device is in a standby mode and selecting the second input buffer when the mode of the semiconductor device is in an active mode[[]]

wherein the control means receives an external reference voltage and compares the external reference voltage with an internal reference voltage and then outputs a control signal to select one of the first and second input buffers.

4. (Original) The input buffer circuit according to claim 3, wherein the first input buffer is a CMOS buffer, and the second input buffer is a differential input buffer.

5. (Currently amended) An input buffer circuit used in a SSTL interface, the input buffer circuit comprising:

a differential buffer for differentially comparing a reference potential with an external input signal and buffering the compared signal;

a CMOS buffer for buffering the external input signal through a CMOS; and

a control section for logically combining an enable signal inputted from an external and a control signal, operating the differential buffer when the control signal is in a normal operation state, and operating the CMOS buffer when an input signal~~, such as a command signal or an address signal o~~ including at least one of a command signal and an address signal, is not [[inputted]] input from an external, and when ~~a predetermined operation such as~~ a refresh operation is performed.

6. (Original) The input buffer circuit according to claim 5, wherein the control section includes a first NAND gate for NANDing the enable signal and the control signal, a second inverter for inverting an output signal of the first NAND

gate and outputting as a control signal of the differential buffer, a first inverter for inverting the control signal, a second NAND gate for NANDing the enable signal and the control signal inverted by the first inverter, and a third inverter for inverting an output signal of the second NAND gate and outputting as an operation control signal of the CMOS buffer.

7. (Original) The input buffer circuit according to claim 5, further comprising a reference potential level detecting circuit which detects a level of the external reference potential and generates the control signal which enables the differential buffer to operate only when the level is maintained in a normal operation range and the CMOS buffer to operate when the level deviates from the normal operation range.

8. (Currently Amended) The input buffer circuit according to claim 7, wherein the reference potential level detecting circuit comprises a first and second reference potential generating section for respectively generating a first and second reference potential to set a normal operation range of the external reference potential, a first comparison section operated by an enable signal inputted from an external to differentially compare the first reference potential with the external reference potential, a second comparison section operated by an enable signal inputted from an external to differentially compare the second reference potential with the external reference potential, and a control signal generating section for logically combining outputs of the first and the second reference potential comparison section, generating a control signal which enables the differential buffer to operate only when the external reference potential is [[located]] between the first reference potential and the second reference potential~~, and the CMOS buffer to operate in other cases~~.

9. (Original) The input buffer circuit according to claim 5, further comprising an input signal potential detecting circuit for generating a control signal which enables the CMOS buffer to operate when a potential of the external input signal fully swings.

10. (Original) The input buffer circuit according to claim 9, wherein the input signal potential detecting circuit comprises a first and a second reference potential generating section for respectively generating a first and a second reference potential Vref2 to understand whether or not the external input signal fully swings, a first comparison section operated by an enable signal inputted from an external to differentially compare the first reference potential with the external input signal, a second comparison section operated by an enable signal inputted from an external to differentially compare the second reference potential with the external input signal, a first latch section for receiving an output signal of the first comparison section, an inverted output signal of the first comparison section, latching the received signals, and outputting a control signal which enables the CMOS buffer to operate when the external input signal fully swings, according as the external input signal fully swings or changes a little, and a second latch section for receiving an output signal of the second comparison section, an inverted output signal of the first comparison section, latching the received signals, and outputting a control signal which enables the CMOS buffer to operate when the external input signal fully swings, according as the external input signal fully swings or changes a little.